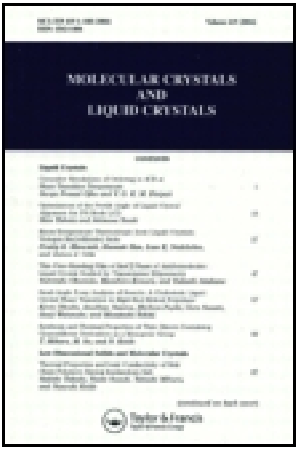

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Admittance Spectroscopic Analysis of Polymer Light Emitting Diodes with the LiF Cathode Buffer Layer

H. M. Kim [a], U. Manna [a], K. S. Jang [a], J. Yi [a], Sunyoung Sohn [b], Keunhee Park [b] & Donggeun Jung [b]

[a] School of Information and Communication Engineering, Sungkyunkwan University, Suwon, Kyunggi-Do, Korea

[b] Department of Physics, Institute of Basic Science, and Brain Korea 21 Physics Research Division, Sungkyunkwan University, Suwon, Korea

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H. M. Kim
U. Manna
K. S. Jang
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School of Information and Communication Engineering, Sungkyunkwan University, Suwon, Kyunggi-Do, Korea

Sunyoung Sohn
Keunhee Park
Donggeun Jung
Department of Physics, Institute of Basic Science, and Brain Korea 21 Physics Research Division, Sungkyunkwan University, Suwon, Korea

Admittance Spectroscopic analysis was applied to study the effect of LiF buffer layer and to model the equivalent circuit for poly(2-methoxy-5-(2′-ethylhexyloxy)-1,4-phenylenevinylene) (MEH-PPV)-based polymer light emitting diodes (PLEDs) with the LiF cathode buffer layer. The single layer device with ITO/MEH-PPV/Al structure can be modeled as a simple combination of two resistors and a capacitor. Insertion of a LiF layer at the Al/MEH-PPV interface shifts the lowest unoccupied molecular orbital (LUMO) level and the vacuum level of the MEH-PPV layer as a result of which the barrier height for electron injection at the Al/MEH-PPV interface is reduced. The admittance spectroscopic analysis of the devices with the LiF cathode buffer layer shows reduction in contact resistance (R_C), parallel resistance (R_P) and increment in parallel capacitance (C_P).

Keywords: admittance spectroscopy; barrier height; LiF buffer layer; polymer light emitting diodes

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Address correspondence to Prof. J. Yi, School of Information and Communication Engineering, Sungkyunkwan University, 300, Chunchun-dong, jangan-Gu, Suwon-city, Kyunggi-Do, 440-746, Republic of Korea (ROK). E-mail: yi@yurim.skku.ac.kr

INTRODUCTION

The reports of Tang *et al*. on efficient organic light emitting diodes (OLEDs) for organic materials based on tris-(8-hydroxyquinoline) aluminum (Alq_3) has drawn the interest for the use of polymer as an emitter in multilayer structure of electroluminescent device [1–2]. In polymer light emitting diodes (PLEDs), both the electron and the hole should be injected efficiently for best device performance. It means that a small injection barrier height at the cathode/organic interface is required. Insertion of an insulating layer between the cathode and the organic layer leads to a significant improvement in the charge injection and electroluminescence output [3]. The enhancement is due to the increased charge carrier density near the cathode/organic interface that results from enhanced electron tunneling, and removal of exciton-quenching gap states that are intrinsic to the cathode/organic interface [4–7]. Insertion of a LiF layer at the cathode/organic interface shifts the lowest unoccupied molecular orbital level and the vacuum level of the organic layer as a result the barrier height for electron injection at the cathode/organic interface is reduced [8].

Admittance Spectroscopy is one of the powerful tools used to study the equivalent circuit models, the charge carrier dynamics, and dielectric properties of organic devices [9]. The single layer device with ITO/MEH-PPV/Al structure can be modeled as a simple parallel combination of resistor and capacitor [10].

In this work, we have applied the admittance spectroscopy analysis to find the effect of LiF cathode buffer layer and to model the equivalent circuit for ITO/MEH-PPV/LiF/Al device structure.

EXPERIMENTAL

Fabrication of PLED

The indium tin oxide (ITO)-coated glass with a sheet resistance of $11\,\Omega$/sq. was used as the anode for PLEDs. For the preparation of PLEDs, the ITO glass was cleaned sequentially in ultrasonic bath of trichloroethylene, acetone, and methanol. Finally, the ITO glass was sonicated in deionized water and then blown dry with N_2 gas. The LiF as the cathode buffer layer was deposited to a thickness of 0.5 nm by thermal evaporation. The emitting material layer (EML) used is of 0.75 wt.% poly(2-methoxy-5-(2′-ethylhexyloxy)-1,4-phenylenevinylene) (MEH-PPV) solution in chlorobenzene. The 80-nm-thick MEH-PPV layer was prepared sequentially by spin coating on the substrate. For the removal of the residual solvent, spin coated MEH-PPV film was baked in vacuum oven for 30 min. The cathode with

0.5-nm-thick LiF and 100-nm-thick aluminum (Al) was deposited by thermal evaporation.

Measurements

The Admittance measurement was carried out by using LF 4192A Impedance analyzer. The amplitude test signal was 50 mV. The measurement frequency was in the range from 10 Hz to 10 MHz. A Keithley 2400 electrometer was used for measuring current density-voltage (J-V) characteristics as a voltage source and current measurement equipment.

RESULTS AND DISCUSSION

The capacitance and conductance were measured for the devices with and without LiF layer in the frequency range of 10 Hz to 10 MHz for zero bias voltage to find the effect of LiF layer. Figure 1 shows the capacitance versus frequency (C-F) characteristics for the device with ITO/MEH-PPV/Al and ITO/MEH-PPV/LiF/Al structures. For the high frequency region, the values of capacitances with and without LiF layer are almost equal, but for the low frequency region, there is an increment in the capacitance with the introduction of the LiF layer, which is related to the enhancement of carrier injection and space charge formed by the injected carriers [11].

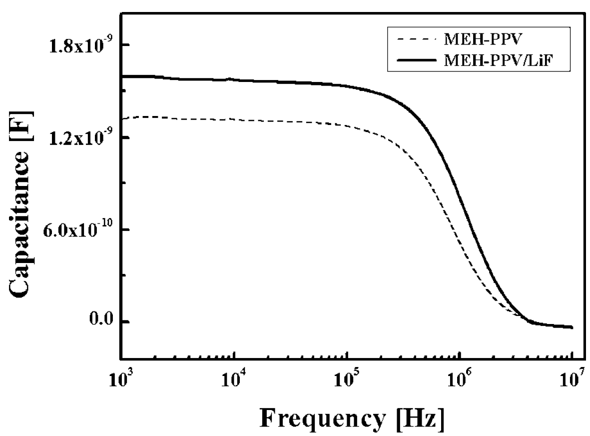


FIGURE 1 Capacitance variation with frequency in the device with and without LiF as a buffer layer between cathode and organic interface.

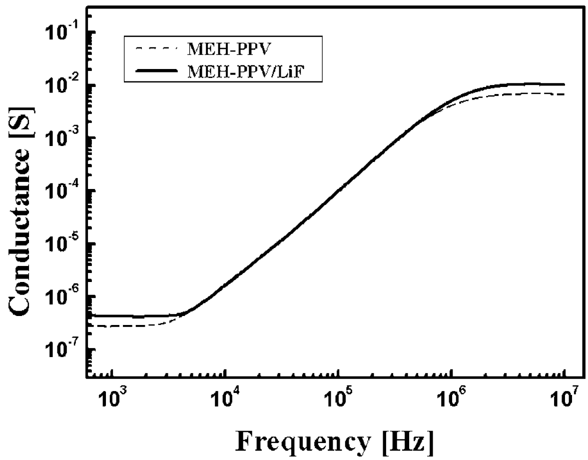


FIGURE 2 Conductance variation with frequency in the device with and without LiF as a buffer layer between cathode and organic interface.

Figure 2 shows that the conductance of the device increases for the low and high frequency region when the LiF layer is inserted into the cathode/organic interface, which is basically caused by carrier injection enhancement, as mentioned early.

For the device modeling, the impedance was measured for the devices with and without LiF layer for a rage of 10 Hz to 10 MHz for zero bias voltage. The results were analyzed by the complex admittance equation [12]

$$Y = \frac{1}{Z} = G + jB = G + jwC = Y' + jY'' \qquad (1)$$

where Y, Z, G, B and C are the admittance, impedance, conductance, susceptance and capacitance of the device, respectively. Figure 3 shows the Cole-Cole plots of the device with and without LiF layer. The horizontal and vertical axes represent the real (Y′) and the imaginary (Y″) parts of the admittance of the devices, respectively.

The equivalent circuit of the devices consists of a parallel resistance (R_P) and capacitor (C_P) network in series with a contact resistance (R_C) as shown in Figure 4.

The values of contact resistance (R_C), parallel resistance (R_P) and increment in parallel capacitance (C_P) extracted from the cole-cole plot for the devices with and without LiF layer is summarized in Table 1.

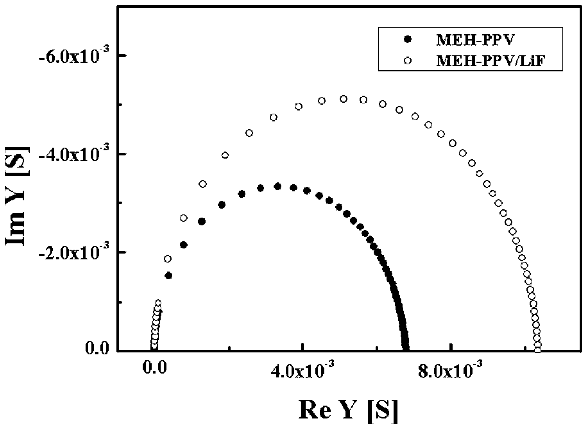


FIGURE 3 Cole-cole plot for the device with and without LiF as a buffer layer between cathode and organic interface.

Fowler-Nordheim tunneling equation is given as [13–15]

$$I = \frac{2.2\,e^3V^2}{8\pi h\Phi_D d^2}\exp\left(-\frac{8\pi d}{2.96\,h_e V}(2m)^{1/2}\Phi_D^{3/2}\right) \tag{2}$$

We can calculate the values of the constants A and k from the Eq. (3).

$$I \propto AF^2 \exp\left(\frac{-k}{F}\right) \tag{3}$$

In order to understand the relation between I and F, we used a generalized Eq. (4).

$$I \propto F^2 \exp\left(\frac{-k}{F}\right) \tag{4}$$

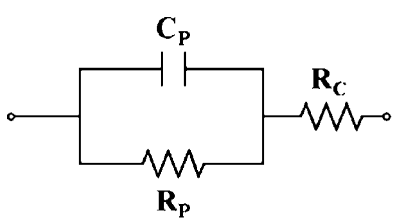
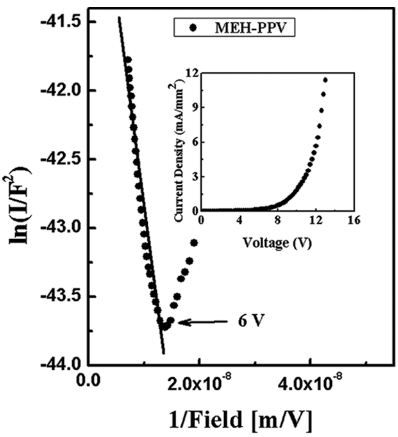


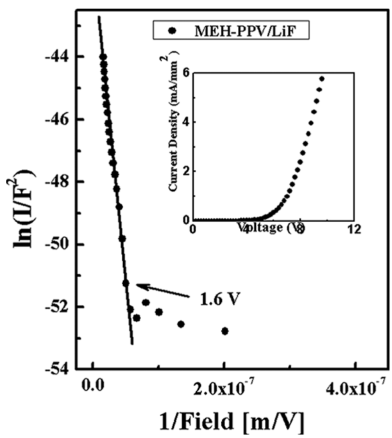
FIGURE 4 Equivalent circuit model for the device.

TABLE 1 Comparison of Values of Resistance and Capacitance for the Device with and without LiF Layer

	Without LiF layer	With LiF layer
R_C (Ω)	147	96.5
R_P (MΩ)	3.7	2.3
C_P (nF)	1.3	1.6



(a)



(b)

FIGURE 5 Fowler-Nordheim tunneling plot (a) without LiF (b) with LiF buffer layer, between cathode and organic interface. The curve in close up shows the current density-voltage (J-V) characteristics of the devices.

Simplifying the Eq. (4). by taking log on both sides, we get the Eq. (5).

$$\ln\left(\frac{I}{F^2}\right) \propto -\frac{k}{F} \tag{5}$$

where I is the current, F is the electric-field strength, and k is a parameter that depends on the barrier shape.

Figure 5 shows the plot of ln (I/F^2) versus $(1/F)$. The curve seems to be very close to linear and the slope of which gives the value of k. The values of k were calculated to be 2.862×10^8 and 2.118×10^8 from the plots of Figures 5(a) and (b) for the case without and with LiF as a buffer layer, respectively. The slope decrease after the insertion of LiF as a buffer layer. Smaller value of k gives lower barrier height [15] as a result of which the turn on voltage of the device becomes lower. The difference in the barrier height ultimately brings change in external quantum efficiency [16] of the device from 0.005% to 0.095% with a net increase of 0.090% as shown in Figure 6.

Insertion of a LiF layer at the Al/MEH-PPV interface shifts the LUMO level and the vacuum level of the MEH-PPV layer, as a result of which the barrier height for electron injection at the Al/MEH-PPV interface is reduced. It leads to the reduction in the driving voltage of the device with LiF layer. The reduction of barrier height is attributed to the increment in C_P and the reduction in driving voltage is

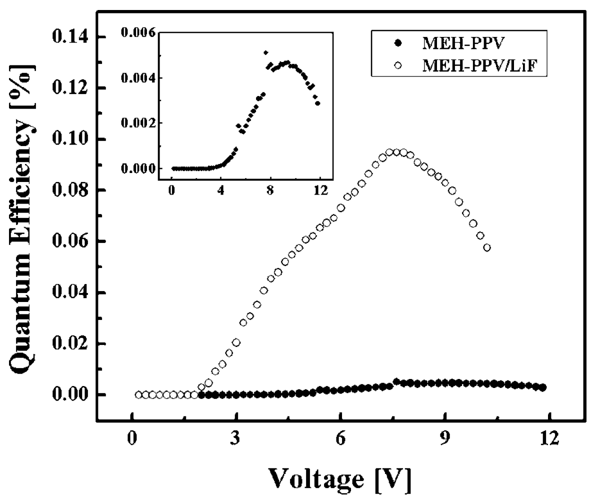


FIGURE 6 Variation in quantum efficiency with bias voltage with and without (close up) LiF as a buffer layer between cathode and organic interface.

attributed to the reduction in the R_P of the device with LiF layer, which is well supported by our admittance measurement.

CONCLUSIONS

The device with the LiF cathode buffer layer at the Al/MEH-PPV interface can be expressed as a simple combination of two resistors and a capacitor with a reduced value of resistance and increased value of capacitance than that of the device without the LiF cathode buffer layer. The lowering of the barrier height in PLEDs with thin LiF layer is attributed to the increment in device capacitance and the lowering of the driving voltage in PLEDs with a thin LiF layer.

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